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C Ebeling, DC Cronquist, P Franklin, C Fisher - Proc. Field Programmable Logic and Applications, 1997 - [heat.vlsilab.iecs.fcu.edu.tw](#)

... processor similar to dening custom **instructions** using writable ... matrixtobe loadedpriortocom- putation, an **extra** RAM is ... is activated, and one **context bit** can ...

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K Denecker, D Van De Ville, F Habils, W Meeus, M ... - Signal Processing: Image Communication, 2002 - Elsevier

... respec- tively, are enlarged to size 16 by adding **extra** ... the transposition of a matrix of  $q \times B$  **bits**. ... to the integer-oriented nature of the **instructions** of a ...

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[\[PS\] Implementing Data Parallel C on a Custom Computing Machine](#)

JD Kim - [mcs.newpaltz.edu](#)

... The daughterboard is responsible for **extra** signal inputs ... on each PE even if the **context bit** is reset. ... the beginning of this phase, a custom **instruction** set for ...

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MP Phillips - 2001 - [ai.mit.edu](#)

... tagged with the pointer (P) and user (U, V) **bits**. **Instruction** memory is read-only. Page-outs are not supported. The only way to get ...

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[Implementation and Analysis of Helper Threads with SSMT](#)

K Asrigo, C Comis, H Shojania - [hassan.shojania.com](#)

... realistic helper threading scenario, a natural **extension** to the ... will make LCU context **instruction** (4) to wake ... Any **extra** code added there was seriously impeding ...

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J Li, K Yu, S Li - 2006 - [freepatentsonline.com](#)

... The **context bit** C1 is also removed to further ... In addition, **extra bits** to describe the regions of ... in the general context of processor-executable **instructions**. ...

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[Method and apparatus for synchronizing a packet based modem supporting multiple X-DSL protocols - all 3 versions »](#)

A Shridhar, TR Ramesh, RS Bajwa, M Eskandari, F ... - US Patent 6,842,429, 2005 - Google Patents

... line equalization, and (c) a host interface between the information **bit** stream and ...  
processes the data in it in accordance with the **instructions** or parameters ...  
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[PS] **Bit Section Instruction Set Extension** of ARM for Embedded Applications

File Format: Adobe PostScript - [View as Text](#)

In addition to the generation of **extra instructions** for packing ... operations in **context of bit** sections with compile time fixed and dy- ...

[www.cs.arizona.edu/people/gupta/research/Publications/Comp/cases02.ps](http://www.cs.arizona.edu/people/gupta/research/Publications/Comp/cases02.ps) -

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[PDF] **Dynamic Coalescing for 16-Bit Instructions**

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of 16-bit code. A new class of AX **instructions** is carefully designed so that. **extra Thumb instructions** can be eliminated at runtime through **instruction** ...

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**Intel reveals new 64-bit server chip** | CNET News.com

The move to add 64-bit **extensions** to the existing x86 architecture is a long ... Among other things, adding 64-bit **instructions** enables support for more ...

[news.com.com/Intel+reveals+new+64-bit+server+chip/2100-1006\\_3-5160169.html](http://news.com.com/Intel+reveals+new+64-bit+server+chip/2100-1006_3-5160169.html) - 52k -

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**Real Machines with 24-bit and 48-bit words**

Microcode **instructions** were 12 **bits** long, two to a 24-bit word. ... It only had three index registers, making available an **extra bit** for indirect addressing ...

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[PDF] **SH-5: the 64-bit superH architecture** - Micro, IEEE

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SHmedia **instruction** encoding uses 6 **bits**. of opcode field with a 4-bit **extension** opcode. available in some formats. The SH-5 contains ...

[ieeexplore.ieee.org/iel5/40/18745/00865864.pdf?arnumber=865864](http://ieeexplore.ieee.org/iel5/40/18745/00865864.pdf?arnumber=865864) -

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then the **extra bit**, forced to a binary 0, blocks the carry. from one byte segment to the next; if the **instruction** oper- ates on word data, then the **extra** ...

[ieeexplore.ieee.org/iel5/6186/16513/00762823.pdf](http://ieeexplore.ieee.org/iel5/6186/16513/00762823.pdf) - Similar pages - [Note this](#)

**Windows XP Professional x64 Edition** - Wikipedia, the free encyclopedia

32-bit (currently most) Windows Explorer **extensions** fail to work (due to the fact ... This is, for example, the **context**-menu options from things such as zip ...

[en.wikipedia.org/wiki/Windows\\_XP\\_Professional\\_x64\\_Edition](http://en.wikipedia.org/wiki/Windows_XP_Professional_x64_Edition) - 40k -

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Convert media **instruction** to SSE/SSE2 **Instructions**. Microsoft Windows for AMD64 will not **context** switch x87, 3Dnow!, MMX for 64-bit. native threads. ...

[www.amd.com/us-en/assets/content\\_type/](http://www.amd.com/us-en/assets/content_type/)

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in the vector, however, has an **extra bit** to hold the mask **bit**. The execution of a vector **instruction** produces no effect on the elements in the destination ...

iacoma.cs.uiuc.edu/iacoma-papers/nmpisa-tech.pdf - Similar pages - Note this

**64-bit computing in theory and practice - The Tech Report - Page 2**

By moving to a 64-bit addressing scheme, the possible address space grows ... of overlapping **instruction set extensions** that aren't entirely necessary or, ...

techreport.com/reviews/2005q1/64-bits/index.x?pg=2 - 23k -

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Relevance scale ☐ ☐ ☐ ☐ ☐**1** [Compiler construction: an advanced course](#)

F. L. Bauer, F. L. De Remer, M. Griffiths, U. Hill, J. J. Horning, C. H. A. Koster, W. M. McKeeman, P. C. Poole, W. M. Waite, G. Goos, J. Hartmanis  
 January 1974 Book

**Publisher:** Springer-Verlag New York, Inc.Full text available: [pdf\(65.62 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [cited by](#)

The Advanced Course took place from March 4 to 15, 1974 and was organized by the Mathematical Institute of the Technical University of Munich and the Leibniz Computing Center of the Bavarian Academy of Sciences, in co-operation with the European Communities, sponsored by the Ministry for Research and Technology of the Federal Republic of Germany and by the European Research Office, London.

**2** [GPGPU: general purpose computation on graphics hardware](#)

David Luebke, Mark Harris, Jens Krüger, Tim Purcell, Naga Govindaraju, Ian Buck, Cliff Woolley, Aaron Lefohn  
 August 2004 **ACM SIGGRAPH 2004 Course Notes SIGGRAPH '04**

**Publisher:** ACM PressFull text available: [pdf\(63.03 MB\)](#) Additional Information: [full citation](#), [abstract](#), [citations](#)

The graphics processor (GPU) on today's commodity video cards has evolved into an extremely powerful and flexible processor. The latest graphics architectures provide tremendous memory bandwidth and computational horsepower, with fully programmable vertex and pixel processing units that support vector operations up to full IEEE floating point precision. High level languages have emerged for graphics hardware, making this computational power accessible. Architecturally, GPUs are highly parallel s ...

**3** [Dynamic coalescing for 16-bit instructions](#)

Arvind Krishnaswamy, Rajiv Gupta  
 February 2005 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 4  
 Issue 1

**Publisher:** ACM PressFull text available: [pdf\(487.89 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

In the embedded domain, memory usage and energy consumption are critical

constraints. Embedded processors such as the ARM and MIPS provide a 16-bit instruction set, (called Thumb in the case of the ARM family of processors), in addition to the 32-bit instruction set to address these concerns. Using 16-bit instructions one can achieve code size reduction and instruction cache energy savings at the cost of performance. This paper presents a novel approach that enhances the performance of 16-bit Thu ...

**Keywords:** 16-bit Thumb ISA, 32-bit ARM ISA, AX instructions, Embedded processor, code size, energy, instruction coalescing, performance

4 Session S3.2: extention and benchmarks: Bit section instruction set extension of ARM for embedded applications



Bengu Li, Rajiv Gupta

October 2002 **Proceedings of the 2002 international conference on Compilers, architecture, and synthesis for embedded systems CASES '02**

**Publisher:** ACM Press

Full text available: pdf(198.13 KB)

Additional Information: full citation, abstract, references, citings, index terms

Programs that manipulate data at subword level, i.e. bit sections within a word, are common place in the embedded domain. Examples of such applications include media processing as well as network processing codes. These applications spend significant amounts of time packing and unpacking narrow width data into memory words. The execution time and memory overhead of packing and unpacking operations can be greatly reduced by providing direct instruction set support for manipulating bit sections. In ...

**Keywords:** bit section operations, multimedia data, network processing

5 Enhancing the performance of 16-bit code using augmenting instructions



Arvind Krishnaswamy, Rajiv Gupta

June 2003 **ACM SIGPLAN Notices , Proceedings of the 2003 ACM SIGPLAN conference on Language, compiler, and tool for embedded systems LCTES '03**, Volume 38 Issue 7

**Publisher:** ACM Press

Full text available: pdf(276.13 KB)

Additional Information: full citation, abstract, references, citings, index terms

In the embedded domain, memory usage and energy consumption are critical constraints. Dual width instruction set embedded processors such as the ARM provide a 16-bit instruction set in addition to the 32-bit instruction set to address these concerns. Using 16-bit instructions one can achieve code size reduction and I-cache energy savings at the cost of performance. We have observed that throughout 16-bit Thumb code there exist Thumb instruction pairs that are equivalent to a single ARM instructi ...

**Keywords:** 16-bit thumb ISA, 32-bit ARM ISA, AX instructions, code size, embedded processor, instruction coalescing, performance

6 The multics system: an examination of its structure

Elliott I. Organick

January 1972 Book

**Publisher:** MIT Press

Full text available: pdf(23.94 MB)

Additional Information: full citation, abstract, references, cited by, index terms

This volume provides an overview of the Multics system developed at M.I.T.--a time-shared, general purpose utility like system with third-generation software. The advantage

that this new system has over its predecessors lies in its expanded capacity to manipulate and file information on several levels and to police and control access to data in its various files. On the invitation of M.I.T.'s Project MAC, Elliott Organick developed over a period of years an explanation of the workings, concep ...

## 7 Anatomy of LISP

John Allen

January 1978 Book

**Publisher:** McGraw-Hill, Inc.

Additional Information: [full citation](#), [abstract](#), [references](#), [cited by](#), [index terms](#)

This text is nominally about LISP and data structures. However, in the process it covers much broader areas of computer science. The author has long felt that the beginning student of computer science has been getting 'a distorted and disjointed picture of the field. In some ways this confusion is natural; the field has been growing at such a rapid rate that few are prepared to be judged experts in all areas of the discipline. The current alternative seems to be to give a few introductory cou ...

## 8 Essays in computing science

C. A. R. Hoare

January 1989 Book

**Publisher:** Prentice-Hall, Inc.

Full text available:  pdf(20.91 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [cited by](#), [review](#)

Charles Antony Richard Hoare is one of the most productive and prolific computer scientists. This volume contains a selection of his published papers. There is a need, as in a Shakespearian Chorus, to offer some apology for what the book manifestly fails to achieve. It is not a complete 'collected works'. Selection between papers of this quality is not easy and, given the book's already considerable size, some difficult decisions as to what to omit have had to be made. Pity the editor weighin ...

## 9 Real-time shading



Marc Olano, Kurt Akeley, John C. Hart, Wolfgang Heidrich, Michael McCool, Jason L. Mitchell, Randi Rost

August 2004 **ACM SIGGRAPH 2004 Course Notes SIGGRAPH '04**

**Publisher:** ACM Press


Full text available:  pdf(7.39 MB) Additional Information: [full citation](#), [abstract](#)

Real-time procedural shading was once seen as a distant dream. When the first version of this course was offered four years ago, real-time shading was possible, but only with one-of-a-kind hardware or by combining the effects of tens to hundreds of rendering passes. Today, almost every new computer comes with graphics hardware capable of interactively executing shaders of thousands to tens of thousands of instructions. This course has been redesigned to address today's real-time shading capabili ...

## 10 Classics in software engineering

January 1979 Divisible Book

**Publisher:** Yourdon Press

Full text available:  pdf(22.45 MB) Additional Information: [full citation](#), [cited by](#), [index terms](#)

## 11 Writing efficient programs

Jon Louis Bentley

January 1982 Book

**Publisher:** Prentice-Hall, Inc.

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The primary task of software engineers is the cost-effective development of maintainable and useful software. There are many secondary problems lurking in that definition. One such problem arises from the term "useful": to be useful in the application at hand, software must often be efficient (that is, use little time or space). The problem we will consider in this book is building efficient software systems.

There are a number of levels at which we may confront the problem of efficient ...

**12** [The theory of parsing, translation, and compiling](#)

Alfred V. Aho, Jeffrey D. Ullman

January 1972 Book

**Publisher:** Prentice-Hall, Inc.

Full text available:  [pdf\(98.28 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

**From volume 1 Preface (See Front Matter for full Preface)**

This book is intended for a one or two semester course in compiling theory at the senior or graduate level. It is a theoretically oriented treatment of a practical subject. Our motivation for making it so is threefold.


(1) In an area as rapidly changing as Computer Science, sound pedagogy demands that courses emphasize ideas, rather than implementation details. It is our hope that the algorithms and concepts presented ...

**13** [The relational model for database management: version 2](#)

E. F. Codd

January 1990 Book

**Publisher:** Addison-Wesley Longman Publishing Co., Inc.

Full text available:  [pdf\(28.61 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#), [review](#)

**From the Preface (See Front Matter for full Preface)**


An important adjunct to precision is a sound theoretical foundation. The relational model is solidly based on two parts of mathematics: firstorder predicate logic and the theory of relations. This book, however, does not dwell on the theoretical foundations, but rather on all the features of the relational model that I now perceive as important for database users, and therefore for DBMS vendors. My perceptions result from 20 y ...

**14** [Cryptography and data security](#)

Dorothy Elizabeth Robling Denning

January 1982 Book

**Publisher:** Addison-Wesley Longman Publishing Co., Inc.

Full text available:  [pdf\(19.47 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)


**From the Preface (See Front Matter for full Preface)**

Electronic computers have evolved from exiguous experimental enterprises in the 1940s to prolific practical data processing systems in the 1980s. As we have come to rely on these systems to process and store data, we have also come to wonder about their ability to protect valuable data.




Data security is the science and study of methods of protecting data in computer and communication systems from unauthorized disclosure ...

15 The elements of nature: interactive and realistic techniques

 Oliver Deussen, David S. Ebert, Ron Fedkiw, F. Kenton Musgrave, Przemyslaw Prusinkiewicz, Doug Roble, Jos Stam, Jerry Tessendorf

August 2004 **ACM SIGGRAPH 2004 Course Notes SIGGRAPH '04**

**Publisher:** ACM Press

Full text available:  pdf(17.65 MB) Additional Information: [full citation](#), [abstract](#)


This updated course on simulating natural phenomena will cover the latest research and production techniques for simulating most of the elements of nature. The presenters will provide movie production, interactive simulation, and research perspectives on the difficult task of photorealistic modeling, rendering, and animation of natural phenomena. The course offers a nice balance of the latest interactive graphics hardware-based simulation techniques and the latest physics-based simulation techni ...

16 Macintosh human interface guidelines

Apple Computer, Inc.

January 1992 Book


**Publisher:** Addison-Wesley Publishing Company

Full text available:  pdf(37.61 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [cited by](#), [index terms](#)

Macintosh Human Interface Guidelines describes the way to create products that optimize the interaction between people and Macintosh computers. It explains the whys and hows of the Macintosh interface in general terms and specific details.

Macintosh Human Interface Guidelines helps you link the philosophy behind the Macintosh interface to the actual implementation of interface elements. Examples from a wide range of Macintosh products show good human interface design, including individ ...

17 Compilation: Adaptive and flexible dictionary code compression for embedded applications

 Mats Brorsson, Mikael Collin

October 2006 **Proceedings of the 2006 international conference on Compilers, architecture and synthesis for embedded systems CASES '06**


**Publisher:** ACM Press

Full text available:  pdf(241.01 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)


Dictionary code compression is a technique where long instructions in the memory are replaced with shorter code words used as index in a table to look up the original instructions. We present a new view of dictionary code compression for moderately high-performance processors for embedded applications. Previous work with dictionary code compression has shown decent performance and energy savings results which we verify with our own measurement that are more thorough than previously published. We ...

**Keywords:** dictionary code compression, fetch path energy, instruction memory bandwidth, instruction profiling, processor architecture

18 Register relocation: flexible contexts for multithreading

 Carl A. Waldspurger, William E. Weihl

May 1993 **ACM SIGARCH Computer Architecture News , Proceedings of the 20th annual international symposium on Computer architecture ISCA '93**, Volume 21 Issue 2


**Publisher:** ACM PressFull text available:  pdf(1.06 MB)Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Multithreading is an important technique that improves processor utilization by allowing computation to be overlapped with the long latency operations that commonly occur in multiprocessor systems. This paper presents register relocation, a new mechanism that efficiently supports flexible partitioning of the register file into variable-size contexts with minimal hardware support. Since the number of registers required by thread contexts varies, this flexibility permits a better utilization ...

**19 Combined performance gains of simple cache protocol extensions**

F. Dahlgren, M. Dubois, P. Stenström

April 1994 **ACM SIGARCH Computer Architecture News , Proceedings of the 21ST annual international symposium on Computer architecture ISCA '94**, Volume 22 Issue 2


**Publisher:** IEEE Computer Society Press, ACM PressFull text available:  pdf(1.22 MB)Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

We consider three simple extensions to directory-based cache coherence protocols in shared-memory multiprocessors. These extensions are aimed at reducing the penalties associated with memory accesses and include a hardware prefetching scheme, a migratory sharing optimization, and a competitive-update mechanism. Since they target different components of the read and write penalties, they can be combined effectively. Detailed architectural simulations using five benchmarks show substantial combined ...

**20 High-level views on low-level representations**

Iavor S. Diatchki, Mark P. Jones, Rebekah Leslie

September 2005 **ACM SIGPLAN Notices , Proceedings of the tenth ACM SIGPLAN international conference on Functional programming ICFP '05**, Volume 40 Issue 9

**Publisher:** ACM PressFull text available:  pdf(176.18 KB)Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This paper explains how the high-level treatment of datatypes in functional languages—using features like constructor functions and pattern matching—can be made to coexist with *bitdata*. We use this term to describe the bit-level representations of data that are required in the construction of many different applications, including operating systems, device drivers, and assemblers. We explain our approach as a combination of two language extensions, each of which could potenti ...

**Keywords:** bit manipulation, bitdata, bitfields, data representation, pattern matching, polymorphism, qualified types, views

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